A HIGH SPEED COLOR VIDEO PRINTER

Background of the Invention

Field of the Invention

The present invention relates to a video printer and, more particularly, to processes and circuits for deriving form data representative of successive lines of a video raster scan, data representative of successive volumes of data extending transversely across lines of the raster scan, and to the printing of the columns of data successively.

Description of Background Art

Currently available video printers can print color image data in successive columns from a color video raster scan, however these printers are slow in operation. Moreover, currently available video printers typically require two line memories.

In additional to the aforementioned problem, the described conventional color video printer has the shortcoming of needing two line memories.

Summary of the Invention

It is therefore, an object of the current invention to provide an improved process and apparatus for printing of color video images.

For the above and other purposes, ~~With a video to~~ overcoming ~~these~~ problems, the present invention provides a ~~contemplates data~~ converter ~~conversion,~~ a memory for storing data representative of at least one field of a raster scan, and means for reading the columns of data from the memory, with the columns of data being output to a printer during respective successive periods associated with the occurrence of successive field periods of the scan.

By use of a data converter, the columns of data for a field of the scan can be read out and printed much more rapidly than in currently available video printers.

Preferably, each column is read out during a respective blanking period associated with each field of the scan, thereby permitting the scan also to be fed to a video monitor, so that printing can be carried out simultaneously with display on the monitor.

Brief Description of the Drawings

A more complete appreciation of the inventions, and many of the attendant advantages thereof, will be readily enjoyed as the same becomes better understood by reference to the

following detailed description when considered in conjunction with the accompanying drawings in which like numbers indicate the same or similar components, wherein:

Figure 1 is a block diagram of a conventional video color printer,

Figure 2 is an explanatory drawing illustrating the sampling process of one frame video signal at the second analog-to-digital converter 26 in Figure 1,

Figure 3 is a timing diagram of the data input-output for the line memory in Figure 1,

Figure 4 is a block diagram showing one embodiment of a high speed color video printer constructed in accordance with the present invention,

Figure 5 is a block diagram showing one embodiment of the data converting means 60 in Figure 4,

Figure 6 is a block diagram showing another embodiment of the data converting means 60 in Figure 4,

Figure 7 is a layout drawing for the memories of Figures 5 and 6, and

Figure 8 is a timing diagram explaining the operation of Figures 4, 5 and 6.

Detailed Description

Figure 1 illustrates a currently available color video printer. The printer has a color difference decoding section with a luminance and color separator 12, a switch 14, and a color difference decoder 16. A digital video data memory section includes a switch 18, analog-to digital converter 20, a frame memory 22, digital-to-analog converter 24, switch 26 and a switching controller 28 operating switches 18, 26. A video monitor signal output section has a chrominance signal decoder 30 which receives color difference signals, and produces

corresponding chrominance signals, an encoder 32, switch 34, and a monostable multivibrator 36. A printer section has switch ~~No. 5~~, 38, a second analog-to-digital converter 40, a line memory 42, a intermediate gradation converting circuit 44, ~~a intermediate gradation converting circuit 44~~ and a thermal print head (i.e., a "TPH") 46.

In use, ~~composite~~ video signals ~~(CVS) r~~eceived from external sources are divided into luminance signals and chrominance signals by the Y/C separator 12. Switch 14 selects either the luminance signals and chrominance signals separated by Y/C separator 12, or an external super video signal (SVS) according to a selection signal S1, and provides an output to color difference decoder 16. Color difference decoder 16 provides color difference by signals (R-Y, B-Y, Y) by decoding luminance signals and chrominance signals selected by switch 14. At this time, switches 18, 26 are connected to terminals 18c, 18b, 26b, 26c, respectively according to the control of switching controller 28. Accordingly, when the ~~terminal~~ terminals 18c, 18a, 26a, 26b of switches 18, 26 are connected under the control of the switching controller 28, the color difference signals B-Y, R-Y, Y from the color difference decoder 16 are converted to digital signals by analog-to-digital converter 20 and are stored in frame memory 22 as a frame (that is, with 2-fields) of video data.

The video data stored in frame memory 22 is read by a control device and is provided to an input port of digital-to-analog converter 24, which converts the video data read from the frame memory 22 into analog signals for chrominance signal decoder 30. Chrominance signal decoder 30 decodes the analog color difference signals to chrominance signals, R(red), G (green), B (blue), and outputs the decoded analog color difference signals to encoder 32 and to switch 38,

respectively in the form of a video scan. Here, encoder 32 encodes and supplies the incoming red, green and blue chrominance ~~signal~~ signals as composite video signals (CVS) to a monitor (not shown) for visual display.

The encoder outputs, now changed into composite video signals, are applied to one input port of switch 34, which receives pedestal level signals at its second input port. Switch 34 is switched by the output of the MMV 36 triggered by the predetermined period of clock ~~(SCLK),~~ (SCLK) signal and outputs the ~~incoming~~ composite video signals or pedestal level signals to the monitor ~~(not shown).~~ When the data of one frame is provided to the monitor, switch 38 selects and outputs the B-color signal of the frame for printing, under the control of selection signals ~~52,~~ 52 to analog-to-digital converter 40.

During the occurrence of the frame, the clock signal (SCLK) is applied to analog-to-digital converter 40 from the first column (that is, the initial position) in each horizontal line. Accordingly, the B-chrominance signal data corresponding to a vertical line, or column, through the first picture point of each row in the frame, is converted into digital data and is stored into line memory 42.

The data stored in line memory is converted to yellow by the intermediate gradation converting circuit 44, and is printed by thermal print head 46. While the data of one vertical line stored in line memory 42 is being printed, the data of the next ~~following~~ frame is provided to the monitor through switch 34. While the data of the next ~~following~~ frame is being provided to the monitor, analog-to-digital converter 40 samples the video signal of each horizontal line to

assemble a second column of data under the control of the clock signal (SCLK). The digital data sampled by analog-to-digital converter 40 is printed by thermal print head 46 as a second column, next to the first column, and further columns are thereafter printed in a similar manner, for each of the following frames.

After approximately 500-600 columns of one frame of the B-chrominance signal have been printed by this method, the G-chrominance signal ~~of the R, G, B chrominance signal~~ is selected by the selection signal 52 applied to switch 38, which is then printed in vertical columns by a similar process to thereby print the color of magenta. When the magenta color printing has been completed, the ~~R-color signal~~ R-chrominance signal is selected by the selection signal 52 applied to switch 38, and the cyan color is printed by a similar process. In this way, the three colors of Y (yellow), M (magenta) and C (cyan) are printed sequentially.

Figure 2 is an explanatory drawing depicting the sampling process for a frame of the video signal achieved by the sampling clock signal (SCLK) applied to ADC 40 in Figure 1. One frame is composed of an odd field shown in a continuous line and an even field depicted as a dotted line. One frame comprises one video screen display.

The chrominance signal is applied sequentially to ADC 40 by selection of switches and when data of one screen (one frame) is displayed on a monitor, an initial sampling clock signal (SCLK) is used to select a first column forming the picture point of each horizonal line. Accordingly, the chrominance signal of a color selected by switch 38 is converted into digital

data by the clock signal (SCLK) with the first column being sampled. Thereafter, when the data of the next frame is displayed on the monitor, the clock signal (SCLK) applied to ADC 40 selects data for the second column.

By the same method as mentioned above, when approximately 500–600 vertical lines of the first chrominance signal have been sampled, the next chrominance signal is selected by switch selections and sampled by the same process explained above. In this way, R, G, B chrominance signal data of one frame is sampled in columns, and stored in line memory 42.

Figure 3 is a timing diagram of data input–output for line memory 42 of the conventional color video printer of Figure 1. Actually, two line memories are needed for printing of one frame video signal in the conventional color video printer. In other words, when one frame of video signal comprising two fields, as is shown in Figure 3A, is scanned, the first line memory receives that data as is illustrated in Figure 3B. When data is written into the first line memory, the second line memory as is shown in Figure 3C reads the data received during a previous frame period. Here, the data input either written into, or read from the line memory during one frame period is column data as explained ~~in the~~ above~~, column data~~. Likewise, when the No. 2 line memory receives column data during one frame period, the No. 1 line memory reads column data already received during a previous frame period and two line memories perform the input and output alternately.

As described above, conventional color video printers print one line during one screen

(one frame) display period. ~~Their~~ printing times, T1, of one color can be listed as follows:

$$T_1 = T_f \times 500 - 600 \text{ line} = 500T_f - 600T_f = 16.5 - 19.8 \text{ (sec)} \quad (1)$$

There T_f is a frame period encompassing 1/30 seconds (33m sec). Therefore, the total printing time Tt in the case of printing 3 colors against R, G, B ~~signal~~ each becomes as below:

$$T_t = T_1 = 49.5 - 59.4 \text{ (sec)} \quad (2)$$

As seen in the foregoing explanation, the conventional color video printers undesirably use around 50 – 60 seconds to print one multi-colored video frame.

Figure 4 is a block diagram of a high speed video color printer constructed in accordance with the principles of the present invention. A luminance-chrominance separator (Y/C separator) 48 inputs ~~composite~~ video signals CVS and outputs separated luminance and chrominance signals. Switch 50 outputs selectively either the luminance signal and chrominance signal from Y/C separator 48, or the luminance signal and chrominance signal of a super video signal SVC, according to the input of the selective signal S1. A decoder 52 separates chrominance signals R1, G1, B1 and the synchronizing signal ~~SYN 1~~ by decoding the luminance signal and chrominance signal from switch 50. Switch 54 outputs selectively the chrominance ~~signal~~ and synchronizing signal of decoder 52, or chrominance signals R2, G2, B2 and synchronizing signal SYN2 received from an external source according to a predetermined control signal S2. An analog-to-digital converter 56 converts the signal from switch 54 into a digital signal.

MPU microprocessor 58 provides control signals S1, S2, S3 according to the user's input

selection and outputs the control signals onto line 58a. Data converter 60 which includes an internal memory, stores chrominance data signal Ri, Gi, Bi converted into digital signals by ADC means 56 according to the control provided by the MPU 58 on the internal memory, outputs the video data in columns to print output ports 63a, 63b, 63c during the line blanking interval of a field period, and outputs the video signals by field, to a display output ~~prot~~ port 61. DAC 62 converts video data output field by field through display output port 61 of the data converter 60, into analog signals. An encoder 64 encodes the output of digital-to-analog converter 62 into composite video signals that are fed to a video monitor (not shown). Switch 66 ~~outputs~~ selectively outputs signals representative of one color from print output ports 63a, 63b, 63c of the data converter 60, under the control of signal S3 from MPU. A ~~line~~ column memory 68 stores one color of video data selected by switch 66, and then performs the printing by output video data during a residual period minus a period which stores video data for one field period. Intermediate gradation converter 70 converts as an intermediate gradation, the data from the ~~above~~ line memory 68. TPH 72 is a printing device which prints the output of intermediate gradation converting means 70. Therefore, when ~~composite~~ video signal ~~CVS~~ VS in Figure 4 is received, Y/C separating means 48 divides ~~that composite~~ the video signal CVS into luminance and chrominance signals. Switch 50 selectively provides luminance and chrominance signals of the ~~composite~~ video signals CVS separated by Y/C separator 48, or the luminance signals and chrominance signals of the ~~composite~~ super video signal ~~CVS~~ SVS, according to the selective signal S1. Decoder 52 outputs the luminance signals and chrominance signals received from switch 50. Switch 54 selectively provides chrominance signals R1, G1, B1 and synchronizing signals SYN1 from decoder 52, or external chrominance signals R2, G2, B2 and ~~the~~ synchronizing signals

SYN2, according to control signal S2. Analog-to-digital converter 56 provides Ri, Gi, Bi, SYNi by converting chrominance signals and synchronizing signals from switch 54, into digital signals. The ~~digitalized~~ digitized data Ri, Gi, Bi (~~digitalized~~ digitized data of R, G, B signals) from analog-to-digital converter 56 are applied to data converter 60.

If the user selects a print mode, MPU 58 is synchronized to the vertical synchronizing signal SYNi of the incoming video signal and outputs a recording mode signal on line 58a for one frame period. The data converter 60 produces recording addresses by way of recording mode signals, and the data corresponding to the recording addresses are recorded into the internal memory for red, green and blue, respectively. When red, green and blue data Ri, Gi, Bi for one frame are stored into the internal memory of data converter 60, MPU 58 outputs print mode signals on line 58a during the usual vertical blanking signals. MPU 58 activates the internal memory of data converter 60 in order to read out data to be printed (as will be explained in more detail hereinafter), and inputs a write signal to line memory 68.

Now, the data converter 60, in response to the print mode signals, generates and applies printing addresses to its internal memory to address data to be printed column by column. Thus, the data converter 60, generates printing addresses for data comprising the first column from ~~(form~~ the first line to the last line by the first row) in the internal memory during the vertical synchronizing 3H and equalizing pulse 3H period of the blanking interval for the first field period. Then, the data converter 60 produces the printing addresses for the data forming the second column, during the vertical synchronizing 3H and equalizing pulse 3H period of the blanking interval for the

second field period. Thereafter, the data converter 60 generates the printing addresses for the third, further ... through the 512th column, so that the data can be addressed in the internal memory.

Therefore, 512 pieces of picture element data of the first vertical line (or column) stored respectively in red, green and blue in the internal memory of data converter 60, are read and provided to print output ports during a 6H period (about 381 μ sec). The access time per a picture element is as follows:

$$6H/512 \text{ row} = \text{about } 740 \text{ n sec.} \quad (3)$$

One vertical line data of red, green and blue Ro, Go, Bo form each internal memory of data converter 60 is fed to the respective terminals 66b, 66c, 66d of switch 66.

Terminal 66a of switch 66 is connected initially to terminal 66d by control signal S3, resulting in only the blue data Bo read from the internal memory of data converter 60 being provided to line memory means 68.

The data recorded in line memory 68, after the elapse of a 6H period, is read during one field period (16.7 m sec) minus the 6H period (about 381 μ sec) (i.e., 16.7 m sec – 381 μ sec = 16.319 m sec), and is provided to the intermediate gradation converter 70. Converter 70 converts the print data by way of intermediate gradation, and applied the converted data to TPH 72 to enable multi-colored printing. Accordingly, one vertical line (or column) of data for one

frame is printed during 16.319 m sec.

Thereafter, MPU 58 outputs a control signal on line 58a after a period of 6H (which is the vertical synchronizing and equalizing pulse period), and uses data converter 60 to operate in a monitoring mode in order to feed video data to the monitor for visual display.

When operated in a monitoring mode by the control signal on line 58a, the data converter 60 produces monitoring addresses for its internal memory. The monitoring addresses generated by data converter 60, produces addresses for conventional interlaced raster scans, reading the data of odd and even fields from the internal memory. Thus, off rows are ~~firstly~~ read from the internal memory, and then even rows are read ~~from the memory.~~ In response to monitoring of addresses, the data converter 60 firstly outputs to the display output port 61, an odd field of data during the field period that remains after the video data has been output to the print output ports 63a, 63b, 63c in one field period, and then, outputs to the display output port the data for the even field.

Red, green and blue data provided to the display output port 61 of data converter 60 are converted into analog signals by digital-to-analog converter 62. Red, green and blue data converted into analog signals are encoded into composite video signals by encoder 64, and then are displayed on the monitor; this causes one frame of video signal now being printed to also be ~~display~~ displayed. After the frame of video signal has been displayed on the monitor, and when the vertical synchronizing signal is received, MPU 58, as mentioned above, provides a control signal

to line 58a, so that the data converter 60 is again operated in a print mode. Then the data converter 60 designates the second column of the internal memory and generates appropriate addresses. In effect, data converter 60 produces addresses reading from the first row up to the 512th row of the second column during the 6H (381 μ sec) period of the blanking signal interval in the two-field period. Therefore, vertical line data for the second column is read out of the respective internal memory of data converter 60.

Then, switch 66 with the terminal 66a and 66d being connected, transmits the second vertical line of data to the line memory 68 and the second vertical line of data is stored in line memory 68. The stored data of the line memory 68 is, as mentioned above, transmitted to thermal print head 72 through the intermediate gradation converter 70 and is printed in about 16 m sec. Accordingly, the vertical line data is read during the 6H period of each field (262.5H) from the internal memory of the data converter 60 which stores the blue color data, and is applied to print output ports 63a, 63b, 63c and printed during the 262.5H-6H period (16.3 m sec).

In other words, all of the vertical line (513 lines) data for blue color (B) stored in the memory in the data converter 60 are transmitted to the line memory 68 through switch 66 for 8.3 seconds which equals a "16.3 m sec x 512 lines" period, and then is printed. When all the vertical line data for the blue color stored in the internal memory of the data converter 60 has been transmitted to the line memory and printed, the terminal 66a of switch 66 is connected to terminal 66c by MPU 58. When switch 66 is operated, MPU 58, by repeating the same operation as mentioned above, outputs vertical line data per each field from the internal memory of data

converter 60 wherein green color data is stored, and then prints the green color data by transmitting it to line memory 68 for 8.3 seconds.

When the transmission of the green color data is completed, terminal 66a of switch 66 is connected to terminal 66b by MPU 58, and by repeating the same operation as mentioned above, red color data recorded in the internal memory of data converter 60 is transmitted to the line memory 68, column by column. Therefore, ~~let's assume that~~ the total printing time T_o for red, R, green, G and blue, B, color data stored in each internal memory of data converter 60 is T_o. ~~Then the~~ following formula for T_o reads as follows:

$$T_o = 16.7 \text{ m sec} \times 512 \times 3 \text{ colors (R, G, B) } 25.6 \text{ sec.} \quad (4)$$

16.7 msec in the above formula ~~is one field period which~~ is needed for scanning 262.5H. A 6H period of the 16.7 msec total printing time T_o is the data read time for the vertical 20 line data and an approximately 16.319 msec period ~~which is a 16.7 msec-6H period~~ represents the period wherein the vertical line data is printed.

As described above, the present invention can print color video images at a high speed, wherein one frame of video data is stored in the internal memory of a data converter means, the frame data is stored in the internal memory of the data converter and transmitted to line memory at a rate of one column per field period, and then printed, and one screen of video signal is visually displayed on a monitor during the printing operation.

Figure 5 is a block diagram showing an embodiment of the data converter 60 of Figure 4. Recording address generator 74 produces sequentially the addresses for recording one frame of video data on the memory. The printing address generator 76 designates one column out of the memory where the video data 20 is stored, by way of a method which designates sequentially the designated columns and sequential addresses of data locations within a designated column. The monitoring address generator 78 generates sequential addresses to read a field of data from the internal memory, to be output sequentially through the display output port 61. The address selector 80 is controlled by MPU 58 to select the addresses generated by the recording address generator 74, the printing address generator 76, or monitoring address generator 78. The No. 1, 2, and 3 dual-port-memories, DPM 82a, 82b and 82c receive the addresses from the address generators 74, 76 or 78 selected by address selector 80, and store the digital color signals Rl, Gl, B1 received from ADC 56, or output the stored color signal data. No. 1, 2, and 3 dual-port memories 82a, 82b, 82c respectively have print output ports 63a, 63b, 63c, and a display output port 61. The display output ports 61 of dual-output memories 82a, 82b, 82c are connected to DAC 62 to be displayed on the monitor after being converted from digital video signals into analog video signals, and the print output ports 63a, 63b, 63c are respectively connected to the switching terminals of No. 3 selector 66. Accordingly, digital Ri, Gi, Bi data from ADC 56 is respectively applied to the input terminals of No. 1, 2, 3 dual-port memories 82a, 82b, 82c. When the recording mode is selected, MPU 58 is synchronized to the vertical synchronizing signal of the input video signal, and applies recording mode signals to line 58a during one frame period. When the recording mode signal from MPU 58 is supplied to the address selector 80 through line 58a, the address selector 80 is toggled and a 20 terminal 80a is connected to a

terminal 80b. When the terminals 80a and 80b of the address selector 80 are connected, ~~the recording address generator means 74 is connected to No. 1, 2, 3 dual-port memories 82a, 82b, 82c and~~ the recording address generated by recording address generator 74 is supplied to No. 1, 2, and 3 dual-port memories 82a, 82b, 82c. No. 1, 2, and 3 dual-port memories 82a, 82b 82c record Ri, Gi, Bi data received according to the recording addresses generated by the recording address generator 74 for the internal memory cells. The addresses generated by recording address generator 74 are ~~so~~ generated ~~as~~ to align the pixel position of the monitor with the same placement position to be stored in the No. 1, 2, and 3 dual-port memories 82a, 82b, 82c.

As described above, when the user selects the print ~~20~~ mode under the condition that one frame each of red, green, blue color data Ri, Gi, Bi is stored in No. 1, 2, 3 dual-port memories 82a, 82b, 82c respectively, MPU 58 generates print mode signals via line 58a during the 6H period which is the vertical synchronizing and equalizing pulse period. Then, the print output ports 63a, 63b, 63c of No. 1, 2, 3 dual-port memories 82a, 82b, 82c ~~connected to No. 3 selector 66 are~~ are selectively enabled. ~~Data~~ stored in No. 1, 2, 3 dual-port memories 82a, 82b, 82c are supplied via ~~No. 3 selector 66 through~~ respective print output ports 63a, 63b, 63c. The printing addresses generated from printing address generator 76 are ~~so~~ generated to designate one column during the first vertical 3H and equalizing pulse 3H interval (from the first row to the last row in the first column), so the data applied according to selector 68 ~~to No. 3 selector 66~~ through print output ports 63a, 63b, 63c at No. 1, 2, 3 dual-port memories 82a, 82b, 82c is output sequentially to define the first column of data. ~~No. 3 selector~~ switch 66 initially outputs only blue color data to line memory 68 during the 6H period. The line memory 68 outputs the first column data of blue color data during a period not

including the aforesaid period in one field period, and is caused to perform printing.

Thereafter, MPU 58 supplies monitoring mode signals to address selector 80 through line 58a when the 6H period, which is the vertical synchronizing and equalizing pulse period, is over. When monitoring mode signal is input, the address selector 80 is switched so that the terminals 80a, 80b ~~and 80c~~ are connected, and monitoring addresses generated by monitoring address generator 78 are written into No. 1, 2, 3 dual-port memories 82a, 82b, 82c. At this moment, addresses generated by monitoring address generator 78 are normal addresses which read odd and even fields of data from No. 1, 2, 3 dual-port memories 82a, 82b, 82c. First, odd fields of data among the data recorded in No. 1, 2, 3 dual-port memories 82a, 82b, 82c are applied to DAC 62 through display output port 61, and then even fields of data are applied. Red, green, and blue color data output to display output port 61 of No. 1, 2, 3 dual-port memories 82a, 82b, 82c of data convertor 60, are converted into analog signals by DAC 62. Red, green, and blue color data converted into analog signals are encoded to provide composite video signals which are applied to a monitor for visual display. Thus, one frame of the video signal now being printed is simultaneously displayed on the monitor. As mentioned above, after the video image is displayed on a monitor, and then, after a vertical synchronizing signal is received, MPU 58 inputs printing mode signals to address selector 80 through line 58a. Terminals 80a and 80c of address selector 80, as described above are connected in response ~~these~~ printing mode signals. Then, the printing address generator 78 sequentially generates address signals for the second column, starting in the first-row, and moving sequentially up to the 512th row. In other words, by reading addresses from the first row through to the 512th row for the second column during

the 6H interval, ~~that is, for~~ 381 microseconds, data for the second column is generated. Accordingly, data for the ~~No. 2~~ column is read from No. 1, 2, and 3 dual-port memories 82a, 82b, 82c, respectively, and then ~~is~~ provided to print output ports 63a, 63b, 63c, ~~respectively.~~

The No. 2 column of data read (*i.e.*, the second column of data) is, ~~as mentioned,~~ read during a 6H interval. At this moment, ~~No. 3 selector~~ 66 outputs blue ~~20~~ color data only to line memory 68 for a 6H interval, and the line memory outputs the second column of blue color data during a period which excludes the 6H interval during one field period in order to perform printing. Accordingly, each vertical line data in No. 3 dual-port memory 82c is read per a 6H interval of each field of 262.5H, and is printed during an 262.5H - 6H ~~interval, that~~ is, during 16.3 milliseconds.

When the printing of blue color data stored in No. 3 dual-port memory 82c is completed, terminals 66a and 66c in ~~No. 3 selector~~ 66 are connected under the control of MPU 58. When terminals 66a and 66c are connected, MPU 58 repeats the same operations as mentioned above, and transmits column data stored in No. 2 dual-port memory 82b to line memory ~~68~~, for each field, and ~~causes the printing of~~ green color data. When the transmission of data stored in No. 2 dual-port memory 82b is completed, MPU 58 connects terminals 66a and 66b in ~~No. 3 selector~~ 66, repeats the same operation, and transmits red color data stored in No. 1 dual-port memory ~~82a~~ to line memory 68 to ~~produce printing~~ of red color data.

Assuming that total print time for R, G, B color data stored respectively in No. 1, 2, and

3 dual-port memories 82a, 82b, 82c is To, ~~which can be stated as~~:

$$T_o = 16.7 \text{ ~~m sec~~ msec} \times 512 \times 3 \text{ colors (R, G, B)} = 25.6 \text{ sec.} \quad (5)$$

In ~~the foregoing formula~~ formula (5), 16.7 ~~m sec~~ msec is the field frequency cycle of a scanning period of 262.5H and a read time for vertical line data during a 6H interval within the 16.7 ~~m sec~~ msec cycle, while an approximately 16.319 ~~m sec~~ msec period, which is a 16.7 ~~m sec~~ msec 6H period is the time when vertical line data is printed.

Figure 6 is a block diagram depicting another embodiment of data converter 60 shown in Figure 4. The data converter means 60 shown in Figure 6 uses a print output port, as explained in the discussion of Figure 5, and memories 88a, 88b, 88c having one output port, thus eliminating No. 1, 2, 3 dual-port memories 82a, 82b, 82c and their associated display output ports. ~~No. 4 selector~~ switch 86 has a print output port 63 and a display output port 61. ~~No.4 selector~~ switch 86 is connected to the output ports of memories 88a, 88b, 88c. Therefore, data read from memories 88a, 88b, 88c output to one output port, is selected by ~~No. 4 selector~~ switch 86 and is output either to ~~No. 3 selector~~ switch 66 or to DAC 62.

The operation of recording, printing and monitoring address generators 74, 76, 78, and the operation of address selector 80 which selectively ~~output~~ outputs addresses generated by address generators 74, 76, and 78, are controlled by MPU 58, ~~and with one principal difference,~~ and are essentially the same operations explained in conjunction with the discussion of Figure 5. The

principal operating difference is that terminals 86a and 86b in ~~No. 4 selector~~ switch 86 are connected during a 6H interval which is the vertical synchronizing and equalizing pulse period of a blanking signal, and terminals 88a and 88c are connected during other periods. Accordingly, memory means 88a, 88b, 88c are connected to ~~No. 3 selector~~ switch 66 during a 6H interval in one field and the data stored in memories 88a, 88b, 88c are read and output via ~~No. 3 selector~~ switch 66.

~~No. 3 selector~~ switch 66 reads one color of chrominance signal data from the data generated during the 6H interval in one field, and outputs that one color data to line memory 68, ~~and causes~~ causing printing to be performed after the 6H period. Terminals 86a and 86c in ~~No. 4 selector~~ switch 86 are connected under the control of MPU 58 at the end of the 6H interval, and video signals are output for display on the monitor's screen by transmitting odd and even fields of data in sequentially read memories 88a, 88b, 88c to digital-to-analog converter 62.

Figure 7 illustrates a layout of one embodiment of one of the memories 88a, 88b, 88c ~~in~~ shown in ~~either~~ Figure 6 or one of the ~~6, or of No. 1, 2, 3~~ dual-port memories 82a, 82b, 82c shown in Figure 5. The layout has a data storage cell ~~20~~ configuration in a corresponding 1:1 relationship to a pixel screen display (not shown). Here, the first row represents the first horizontal line, while the first column is the data of the first pixel for each line.

Accordingly, the data received from analog-to-digital converter 56 ~~by via the~~ having recording addresses generated ~~normally~~ from recording address generator 74 shown in ~~the circuit illustrated in either~~ Figure 5 or in ~~Figure 6~~ is, as depicted in Figure 7, recorded in the internal memory cell

with the same position as the pixel position on the visual display screen of a monitor. For instance, the data of 1^1, 2^1, 3^1, 4^1,....., 512^1, in a screen is stored in the first row domain of the memory layout, and on the second row domain, data of 1^2, 2^2, 3^2, 4^2,....., 512^2 is stored.

In the foregoing explanation, the number represents the position of rows while the exponent of the number shows the column position. Therefore, when changed to recording mode, Ri, Gi, Bi color data is stored in the memory layout of Figure 7 in an arrangement with each address having a corresponding relation to screen pixel position of the visual display.

When a print mode is selected for a frame of red, green or blue color, data Ri, Gi, Bi is stored in a respective memory, and a vertical one-line of data is read in 1^1, 1^2, 1^3, 1^4,....., 1^{512} order by the printing address generated during the 6H interval which is the vertical synchronizing and equalizing pulse period.

At this moment, 512 pieces of pixel data D_1 from the first vertical line memory are read during the 6H interval, approximately 381 μsec. Therefore, the access time per pixel is ~~around~~ 740 n sec. (6H/512 rows = 740 n sec, where 6H is ~~around~~ 381 μ sec). Afterwards, pixel data D_2 from the second vertical line memory is read in 2^1, 2^2, 2^3 2^4,....., 2^{512} order during a second 6H interval that is the next vertical synchronizing and equalizing pulse period. In this way, the data D_3, D_4, ..., D_{512} of the vertical 3rd, 4th, ..., and 512th lines is read. Meanwhile, the data recorded in memory is read by the monitoring addresses generating from monitoring address generator 78, with odd field data read out of respective memory cells first and then even field

data read. In other words, after the first row data of the 1^1, 2^1, 3^1, 4^1, ..., 512^1 cells, the third row data of the 1^3, 2^3, 3^3, 4^3, ..., 512^3 cells and other odd field data of 5th, 7th, 9th.... 512th rows recorded in respective memory cell rows are read, then the second row data of the 1^2, 2^2, 3^2, 4^2, ..., 512^2 cells, the fourth row data of the 1^4, 2^4, 3^4, 4^4, ..., 512^4 cells, and other even field data of the 6th, 8th, 10th, ..., and 512th rows of cells are read to the parallel ports.

As noted above, when the odd and even field data is read from respective memory cells where red, green, and blue data is stored, and is sequentially output, the one frame of video signal currently being printed is also being displayed.

Figure 8 provides in the patterns of waveforms (A), (B), (C), (D) and (E), a timing diagram explaining the operation of the circuit sections shown in Figures 4, 5, and 6. The pattern of Figure 8(A) is a timing diagram of a composite video signal, namely a timing diagram showing a composite video signal for one field. Accordingly, one field of a composite video signal covers 262.5H and includes a blanking signal 20H and video signals 262.5H – 20H. A blanking signal of 20H in turn, includes an equalizing pulse of 5H or 6H (in order to distinguish odd fields from even fields, a distinction of 5H and 6H is given), and 3H of vertical synchronizing pulses.

The pattern of Figure 8(B) illustrates a timing diagram of a data output enable pulse for either memories 82a, 82b, and 82c, or 88a, 88b, 88c, wherein the output port of memories 82a, 82b, 82c, or 88a, 88b, 88c, connected to ~~No. 3 selector~~ switch 66 is enabled during 6H of vertical

synchronizing and equalizing pulse period.

One color of one vertical line (*i.e.*, one column) of data of blue, green or red is output through ~~No. 3 selector~~ switch 66 during the 6H period (63.5 x 6 = 381 μ sec) during which the output port of memories 82a, 82b, 82c, or 88a, 88b, 88c, has been enabled. Since 512 pieces of pixel data D_1 for the first vertical line of memories 82a, 82b, 82c, or 88a, 88b, 88c, are read during the 6H period of approximately 381 μ sec, an access time per ~~a pixel is around~~ pixel is approximately 740 nano-seconds. In other words,

$$6H/512 \text{ rows} = 740 \text{ n sec}, \tag{6}$$

where 6H equals about 381 μ sec.

The pattern of Figure 8(C) is a timing diagram for a write/read enable pulse of line memory 68. As described in conjunction with the discussion of the pattern of Figure 8(B), line memory 68 stores chrominance signal data of a column of data (one color of one vertical line) which is input through ~~No. 3 selector~~ switch 66 during a 6H period; the particular color depends upon which output port of memories 82a, 82b, 82c, or 88a, 88b, 88c, is enabled. After ~~elapse of~~ the 6H period, line memory 68 reads the chrominance digital data for the stored column during a period of:

$$262.5H - 6H = \text{~~256H~~ } 256.H \tag{7}$$

$$(16.7 \text{ m sec} - 381 \text{ m sec} = 16.319 \text{ m sec}). \tag{8}$$

The pattern of Figure 8(D) provides a timing diagram of the printing period. More

precisely, a timing diagram for the printing period of one color of one vertical line, or column, of the red, green or blue colors. As noted in Figure 8(C), a column of chrominance signal data read from line memory means 68 is read during a period of 262.5H – 6H = 256.5H, where (16.7 ~~m sec~~ – 381 ~~μ seconds~~ = 16.319 milliseconds) and is printed by thermal print head 72 through the intermediate gradation converter 70. In this way, one column of frame data is printed during 16.319 milliseconds.

The pattern of Figure 8(E) provides a timing diagram showing a monitoring enable period, and more precisely, a timing diagram illustrating a period for displaying one frame (*i.e.*, one screen) of video data.

As was noted in the discussion of Figures 8(C) and 8(D), one frame of video data is displayed whilst being printed, *i.e.*, during a period when column data in the line memory 68 is read and printed. In other words, the data for the red, green and blue colors is output, in parallel, to digital-to-analog converter 62, and converted into an analog signal. This parallel analog data is encoded by encoder 64 as a composite video signal, and is output to the monitor, so that one frame of video signal currently being printed is also being displayed.

As explained in the discussion of Figure 8, as one color of column data is printed during one field period, ~~that is, during~~ 16.7 milliseconds, and if three colors having 512 columns respectively are to be printed, the total time ~~to be spent~~ for printing T_0 becomes:

T_o = 16.7 ~~m sec~~ msec x 512 x 3 colors (R, G, B) = 25.6 seconds. (9)

As was explained in the foregoing paragraphs, the described embodiment of a video printer constructed according to the principles of the present invention can print color video images at a high speed by reading video data stored in memory during a 6H interval in one field corresponding to a vertical synchronizing and equalizing pulse period, ~~by~~ storing ~~that~~ the video data in a line memory, ~~by~~ and reading and printing ~~that~~ the video data stored in line memory during the remainder of the field period (which excludes the 6H of vertical synchronizing and equalizing pulse period) within a shortened printing time.